

**Faculty of Engineering and Technology**

**Electrical and Computer Engineering Department**

**Digital Systems ENCS2340**

**Verilog HDL Project**

**Prepared by:**

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**Section: 3.**

**Date: 1/1/2022.**

# **Abstract**

**The aim :**

**Is to design 3 circuits together (9’s complement, BCD adder, quadruple 2x1 mux), and the system working as BCD adder-subtractor circuit.**

**And know how the system works.**

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**1- 9's complement------------------------------------------------------------------------------------------page 1-3**

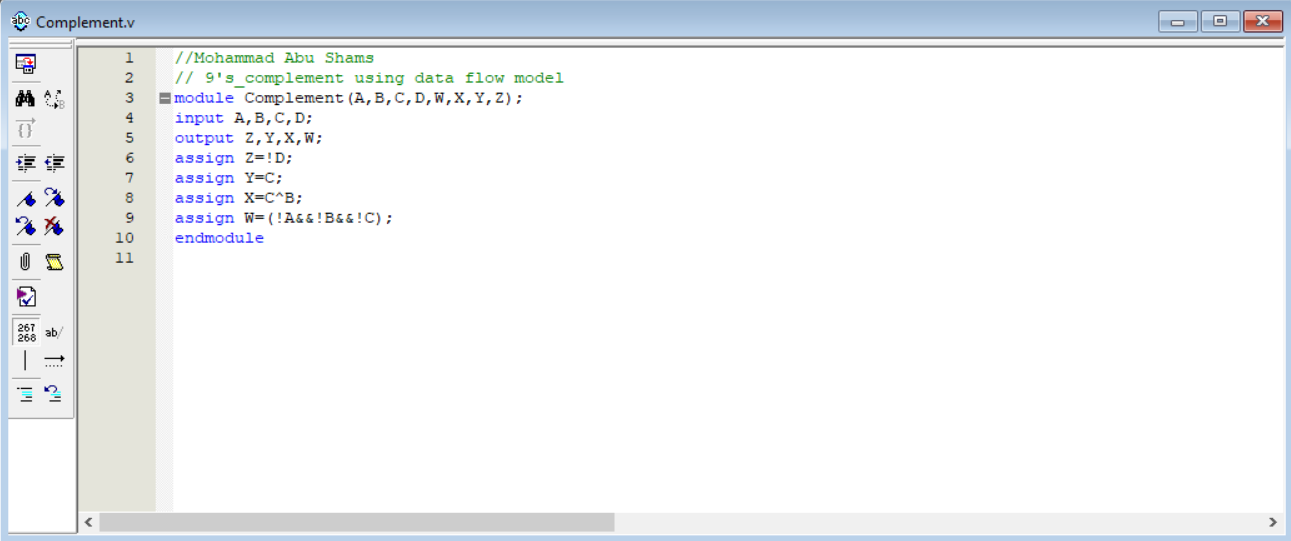
**2-BCD adder -----------------------------------------------------------------------------------------------page 4-5**

**3- Quadruple 2x1 MUX ---------------------------------------------------------------------------------page 6-7**

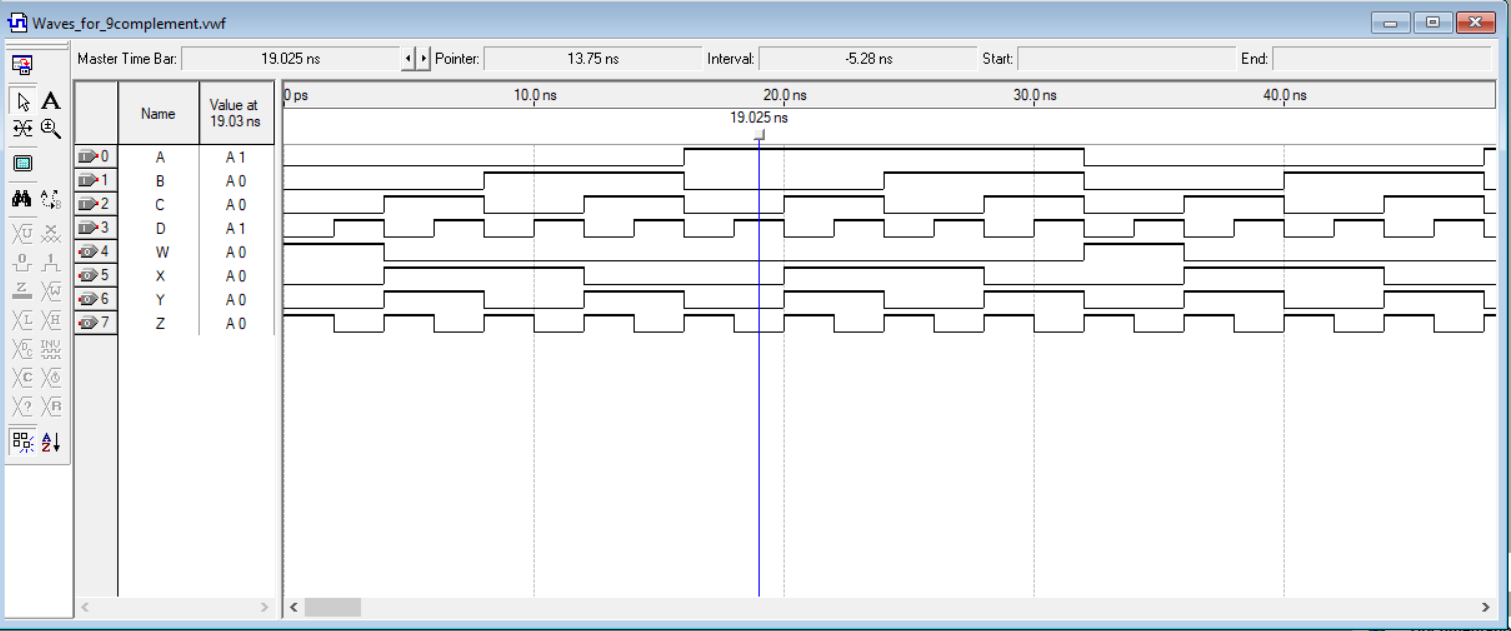
**4- All circuits---------------------------------------------------------------------------------------------page 8-9**

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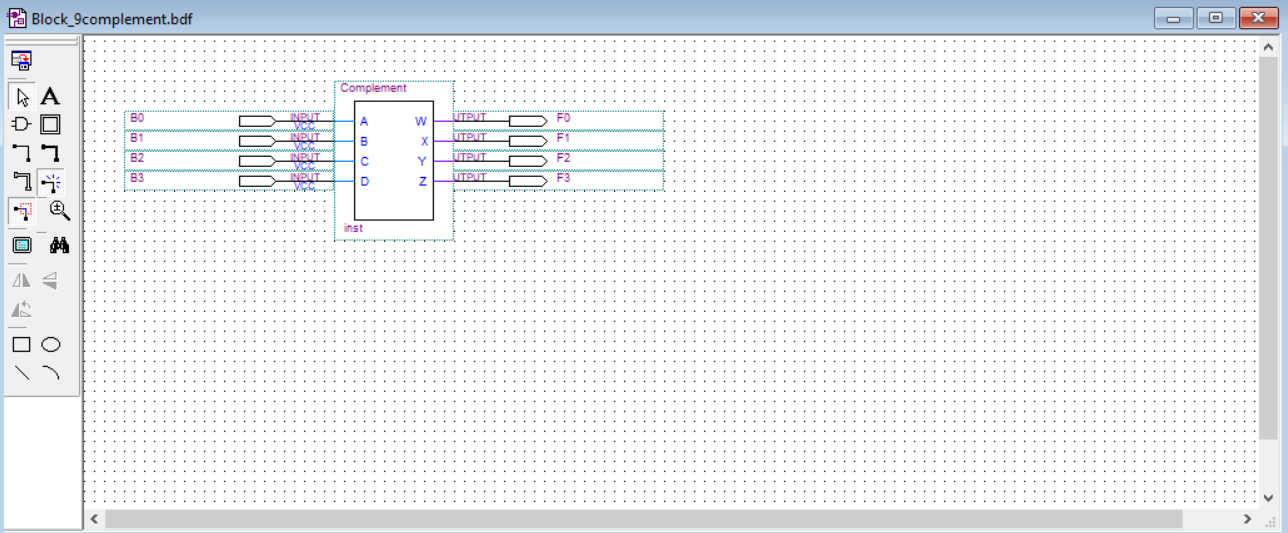
**9’s complement using data flow model.**



**Waves for 9’s complement.**



**Block diagram for 9’s complement.**



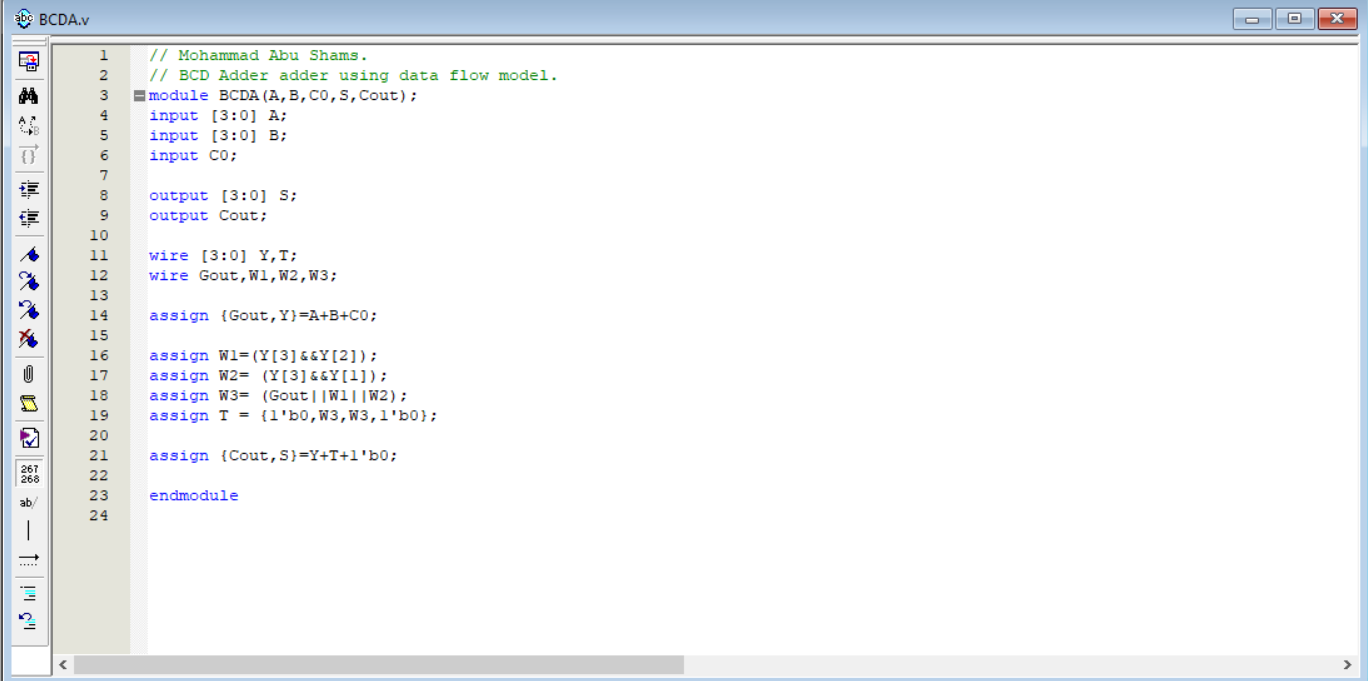
**I designed circuit 9’s complement, it has 4 inputs and 4 outputs.**

**For example if the input equal( 3 Decimal ) which equal ( 0011 in binary ), the output must be ( 9-3=6 Decimal )which equal ( 0110 in binary ) ,, etc……………….**

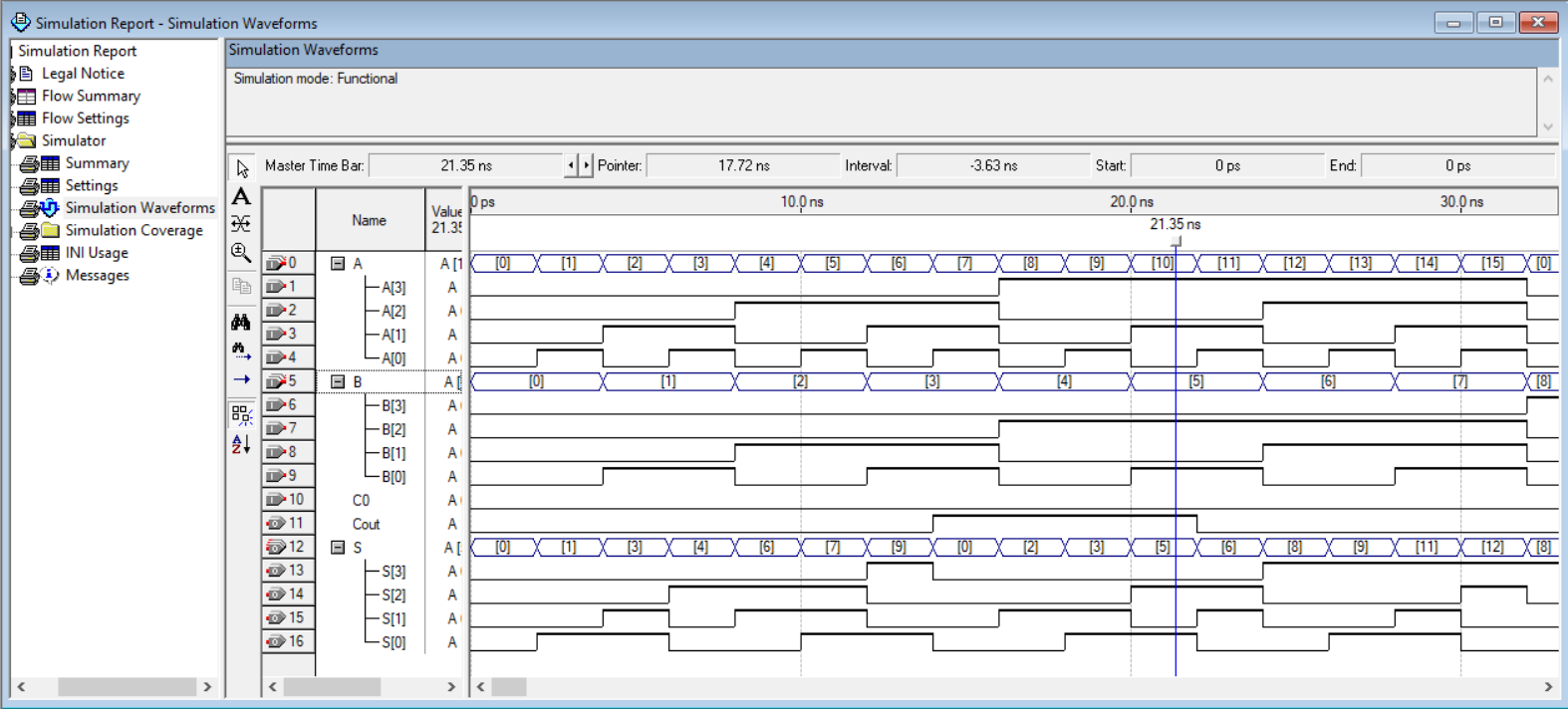
**Truth Table:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0** | **0** | **0** | **0** |  | **1** | **0** | **0** | **1** |
| **0** | **0** | **0** | **1** |  | **1** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** |  | **0** | **1** | **1** | **1** |
| **0** | **0** | **1** | **1** |  | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** |  | **0** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** |  | **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** |  | **0** | **0** | **1** | **1** |
| **0** | **1** | **1** | **1** |  | **0** | **0** | **1** | **0** |
| **1** | **0** | **0** | **0** |  | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** |  | **0** | **0** | **0** | **0** |
| **x** | **x** | **x** | **x** |  | **x** | **x** | **x** | **x** |
| **x** | **x** | **x** | **x** |  | **x** | **x** | **x** | **x** |
| **x** | **x** | **x** | **x** |  | **x** | **x** | **x** | **x** |
| **x** | **x** | **x** | **x** |  | **x** | **x** | **x** | **x** |
| **x** | **x** | **x** | **x** |  | **x** | **x** | **x** | **x** |
| **x** | **x** | **x** | **x** |  | **x** | **x** | **x** | **x** |

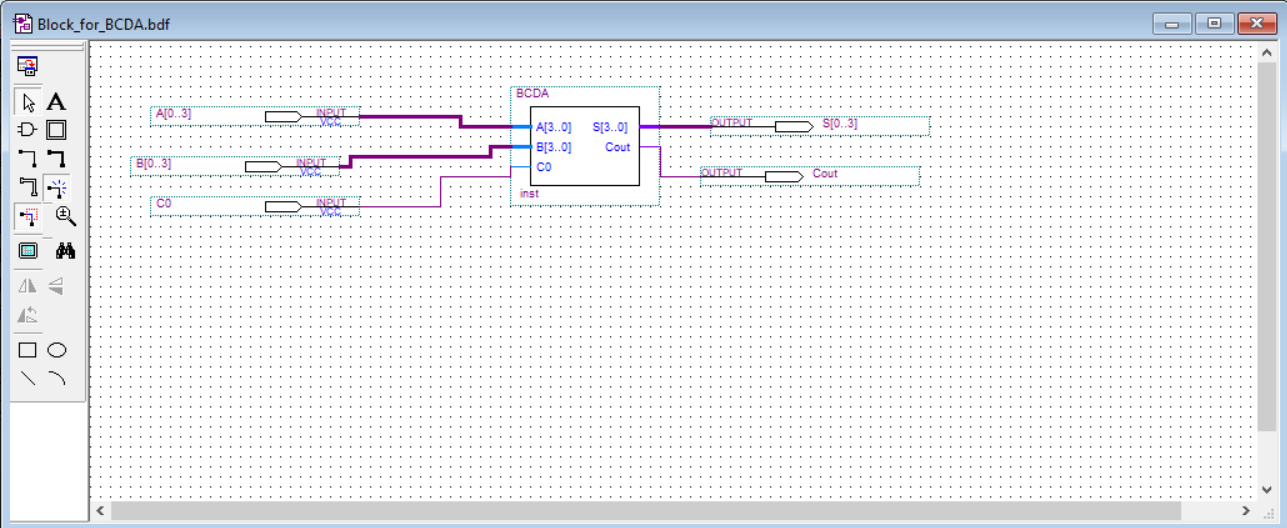
**BCD adder using data flow model.**



**Waves for BCD adder.**

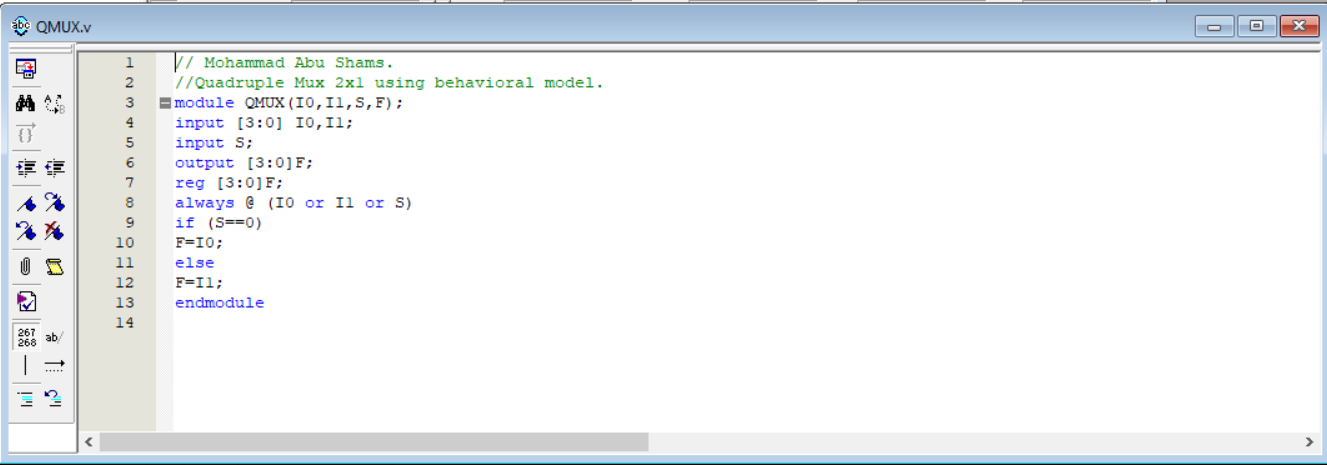


**Block Diagram for BCD adder.**

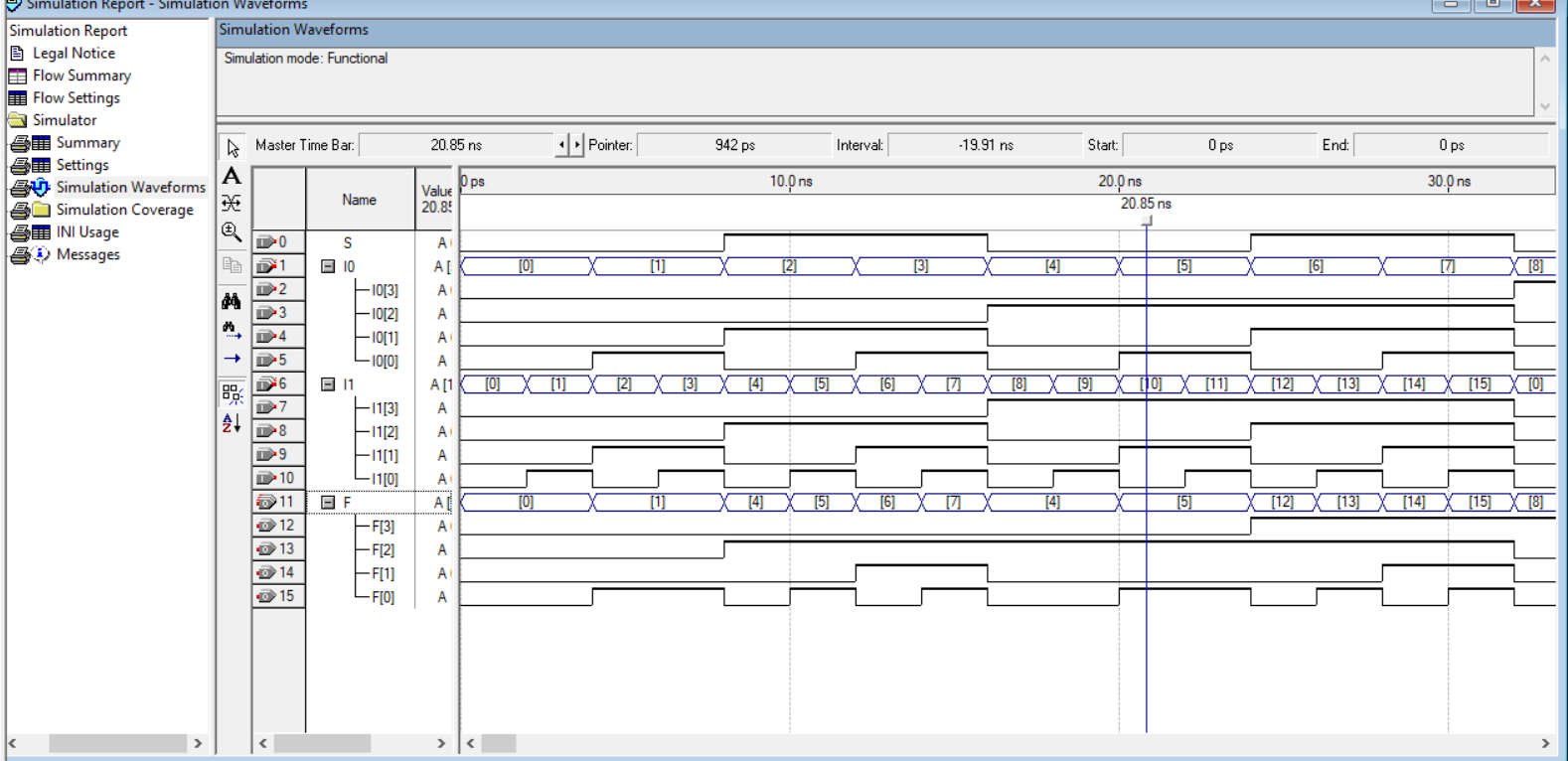


**In BCD Adder, it contains two 4 bit binary adder, C0 equal 0 because it is adder, we add two numbers, if the sum >9, must add (6 in decimal) which equal (0110 in binary).**

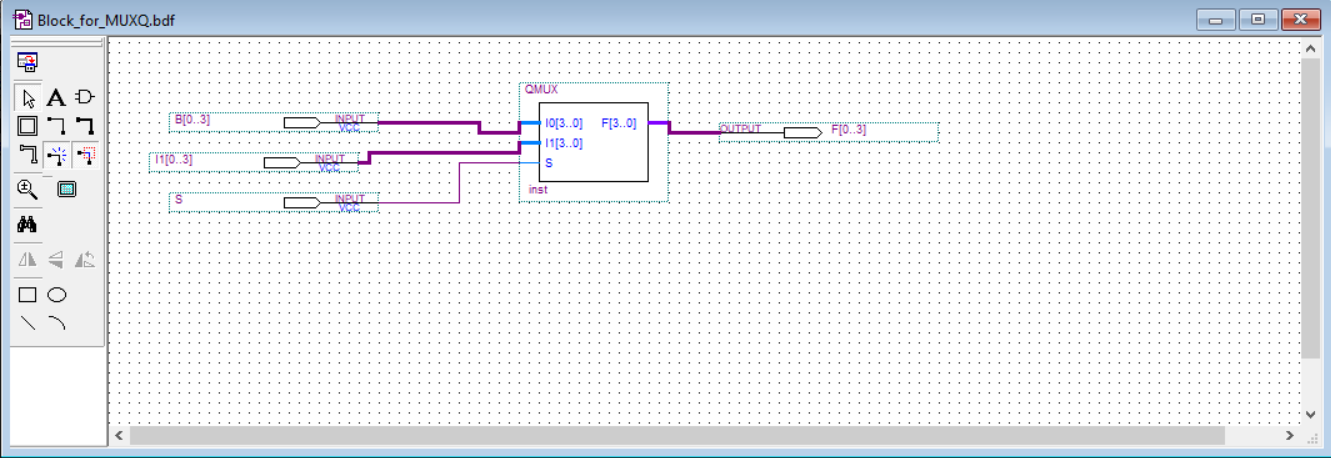
**Quadruple 2x1 MUX using behavioral model.**

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**Waves for Quadruple 2x1 MUX.**

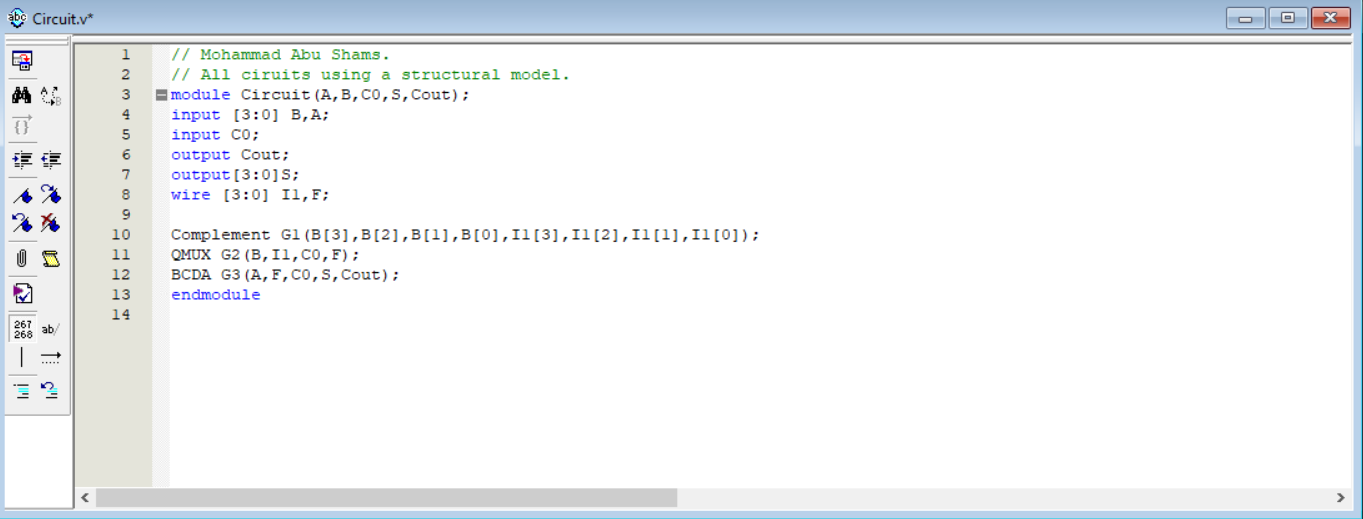


**Block diagram for Quadruple 2x1 MUX .**

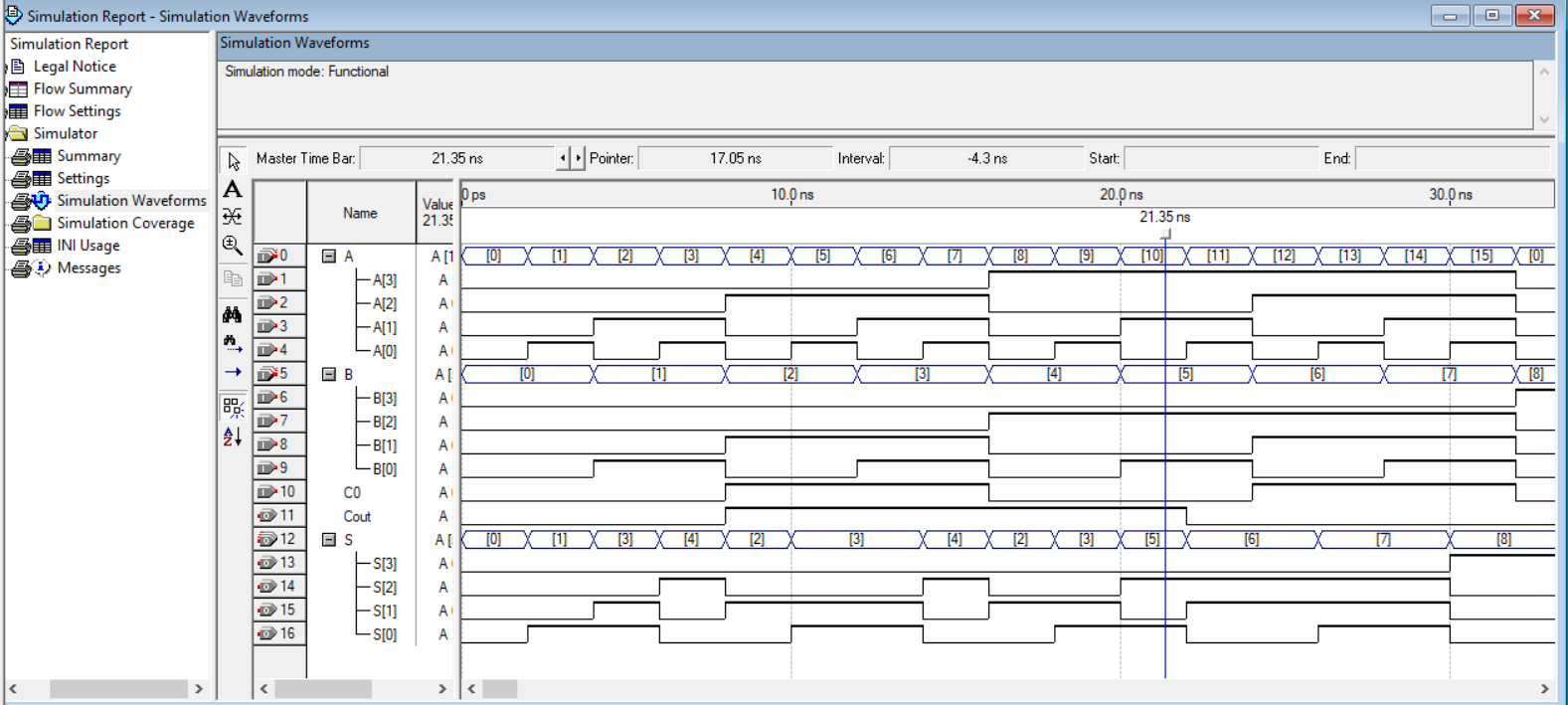
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**I designed a Quaqruple 2x1 MUX, if the selection which is the same with C0 equal 0, then the output which is an array equal the first input which is an array. Otherwise, if C0 equal 1, then the output which is an array equal the second input which is an array.**

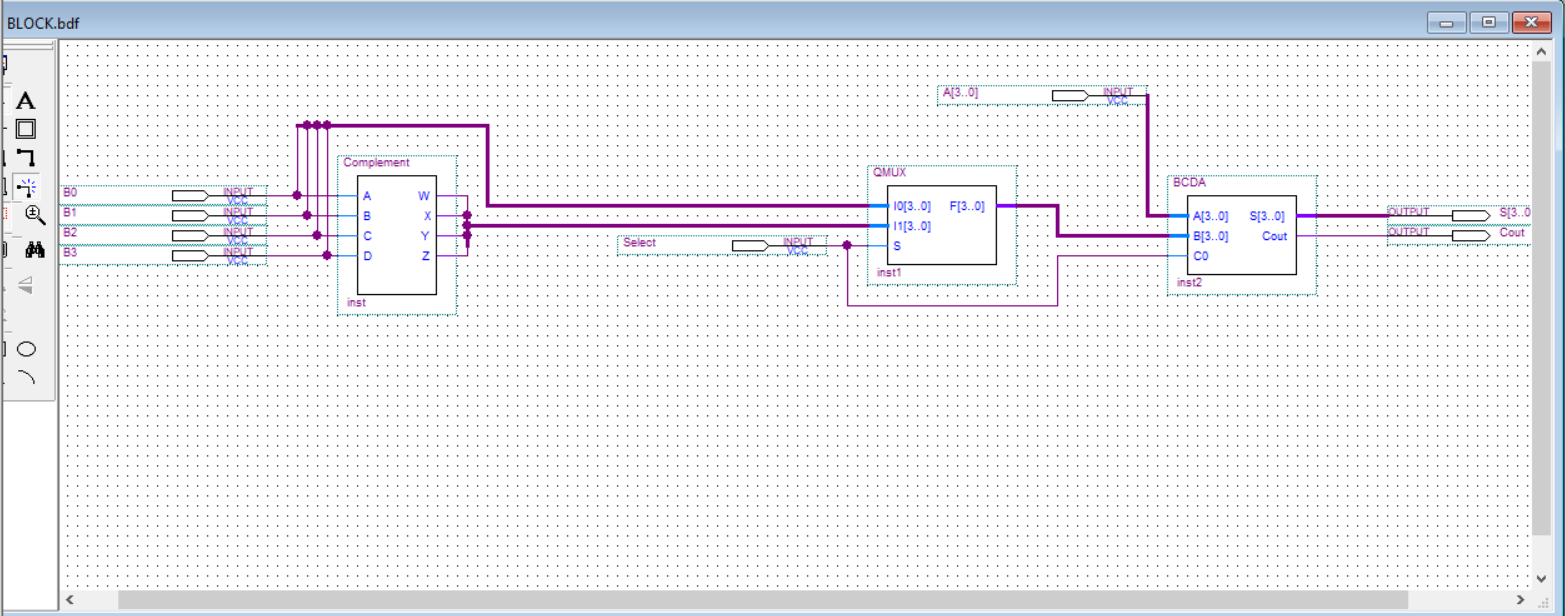
**All circuits using structural model.**

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**Waves for All circuits.**

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**Block diagram for all circuits.**

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**I designed all circuits together, I called BCD adder and mux and 9’s complement, which works together as a photo in the project, the system work as addition when the selection (C0) equal 0, and work subtraction when selection (C0) equal 1.**

**Conculsion :**

**The system works perfectly.**

**THE END**